Atty. Docket No. OF03P212/US
Serial No: 10/733,884

Amendments to the Claims

Please cancel claims 3-4 without prejudice, and amend claim 1 as follows:

1. (Currently Amended) A method of manufacturing a semiconductor device, comprising:

forming a first conductive line on a semiconductor substrate;

forming an insulating layer on the semiconductor substrate and the first conductive line;

forming a first photoresist pattern on the insulating layer, in order to expose parts of the insulating layer where a plurality of via holes will be formed;

using the first photoresist pattern as an etching mask, etching the parts of the insulating layer where [a] the plurality of via holes will be formed to a certain thickness so as not to expose the first conductive line;

forming a second photoresist pattern on the insulating layer, in order to expose parts of the insulating layer where each via hole will be formed;

using the second photoresist pattern as an etching mask, selectively etching a plurality of via holes in each of said parts of the insulating layer in order to expose the first conductive line;

forming a third photoresist pattern on the insulating layer in order to expose parts of the insulating layer where the trenches will be formed;

using the third photoresist pattern as an etching mask, etching trenches in the insulating layer to a certain thickness;

forming a metal barrier the insulating layer and in the via holes; and

forming a plug by depositing a conductive layer sufficiently to fill the via holes, and then planarizing the conductive layer until the conductive layer is substantially coplanar with the insulating layer.

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Previously Presented) The method of claim 1, wherein the first conductive line comprises copper.

6. (Previously Presented) The method of claim 1, wherein the conductive layer and the plug comprise copper.

7. (Previously Presented) The method of claim 6, wherein forming the plug and depositing the conductive layer comprises depositing a copper seed layer by physical vapor deposition (PVD) and forming a copper bulk layer on the copper seed layer by electroplating.

8. (Previously Presented) The method of claim 1, wherein forming the first conductive line comprises sputtering a metal layer, patterning the metal layer using photolithography, and etching the metal layer.

9. (Previously Presented) The method of claim 1, wherein each plurality of via holes has a combined width equal to a width of a corresponding insulating layer part.

10. (Previously Presented) A method of manufacturing a semiconductor device, comprising:

etching a plurality of via holes in each of a plurality of parts of an insulating layer, each plurality of via holes exposing a conductive line on a semiconductor substrate;

etching trenches in the insulating layer to a certain thickness, each of said trenches enabling electrical connection of a subsequently formed conductive layer through a corresponding plurality of via holes to the exposed conductive line;

forming a metal barrier on the insulating layer and in the via holes and trenches;

depositing a conductive layer in the via holes and trenches sufficiently to fill the via holes and trenches; and

planarizing the conductive layer until the conductive layer is substantially coplanar with the insulating layer.

11. (Previously Presented) The method of claim 10, wherein the trenches are etched before the plurality of via holes are etched.

12. (Previously Presented) The method of claim 10, wherein the plurality of via holes has a combined width equal to a width of a corresponding insulating layer part.

13. (Previously Presented) The method of claim 10, further comprising forming the first conductive line by sputtering a metal layer, patterning the metal layer using photolithography, and etching the metal layer.

14. (Previously Presented) The method of claim 10, wherein the conductive layer and the plug comprise copper.

15. (Previously Presented) The method of claim 14, wherein forming the plug and depositing the conductive layer comprises depositing a copper seed layer by physical vapor deposition (PVD) and forming a copper bulk layer on the copper seed layer by electroplating.

16. (Withdrawn) A semiconductor device, comprising:

a first conductive line on a semiconductor substrate;

an insulating layer on the semiconductor substrate and the first conductive line;

a plurality of via holes in each of a plurality of parts of the insulating layer, each of the plurality of via holes exposing the first conductive line, and each of the parts of the insulating layer other than the via holes having a certain thickness greater than zero but less than the insulating layer thickness;

trenches in the insulating layer having a certain depth;

a metal barrier lining the insulating layer and the via holes; and

a plug and a conductive layer filling the via holes, the conductive layer being substantially coplanar with the insulating layer.

17. (Withdrawn) The semiconductor device of claim 16, wherein the first conductive line comprises copper.

18. (Withdrawn) The semiconductor device of claim 16, wherein the conductive layer and the plug comprise copper.

19. (Withdrawn) The semiconductor device of claim 16, wherein the metal barrier comprises Ti, TiN, Ta or TaN.

20. (Withdrawn) The semiconductor device of claim 16, wherein the insulating layer comprises silicon oxide (SiO_2).

21. (Withdrawn) The semiconductor device of claim 16, wherein each of the plurality of via holes has a width equal to a width of a corresponding insulating layer part.

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Election of Species and Restriction Requirement

Applicant has elected, with traverse, Group I, Claims 1 and 3-9, drawn to a method of manufacturing a semiconductor device, and (also with traverse) Group A, Claims 1 and 3-9, directed to a method that comprises etching parts of the insulating layer where a plurality of via holes will be formed to a certain thickness so as not to expose the first conductive line.

Restriction has been required as follows:

Group I: Claims 1 and 3-15, drawn to a method of manufacturing a semiconductor device; and

Group II: Claims 16-21, drawn to a semiconductor device.

Restriction is proper only when the groups of claims are (A) independent or distinct as claimed, and (B) there is a serious burden on the Examiner (M.P.E.P. § 803). Claims are independent when there is no disclosed relationship between them; for example, a process and an apparatus that is incapable of being used in practicing the process (M.P.E.P. § 802.01). Claims are distinct when they are related as disclosed, but are capable of separate manufacture, use or sale as claimed, AND ARE PATENTABLE (novel and unobvious) OVER EACH OTHER (M.P.E.P. § 802.01; emphasis in original). Examiners must provide reasons and/or examples in support of their conclusions (M.P.E.P. § 803).

In this case, no plausible evidence or reasoning has been provided to support the conclusion that Groups I and II are distinct. Although the example that the product as claimed can be made by another, materially different process such as etching via holes exposing the first conductive layer followed by etching the parts of the insulating layer to a certain thickness, it is not clear that such a process is plausible. In Group I, the via holes are formed in the etched parts of the insulating layer, and trenches are also formed in the insulating layer. No evidence or reasoning has been provided to demonstrate that if the via holes are formed first, one could or would later etch both (a) the corresponding parts of the insulating layer where the via holes are formed and (b) the trenches. Without any examples or reasoning that the materially different

process provided in support of restriction is plausible, the materially different process provided simply does not support the conclusion of distinctness between Groups I and II.

As a result, the burden of persuasion has not been met with regard to providing adequate reasons and/or examples in support of the conclusion of distinctness. Thus, the Restriction Requirement is improper and should be withdrawn.

An election of a single, patentably distinct species of the claimed invention has also been required as follows:

Group A: Claims 1 and 3-9, directed to a method in which a plurality of parts of an insulating layer are recessed into the insulating layer; and

Group II: Claims 10-15, directed to a method in which a plurality of parts of an insulating layer are not so limited.

Applicant has elected Group A, with traverse. In view of the above amendment, Claims 1 and 5-9 read on the elected species.

In this case, no reason or example has been provided at all to support the requirement to elect a species. The burden is on the Examiner to provide a reason or example in support of the requirement to elect a species:

> "The particular reasons relied on by the (E)xaminer for holding that the inventions as claimed are either independent or distinct should be concisely stated. A mere statement of conclusion is inadequate. The reasons upon which the conclusion is based should be given." M.P.E.P. § 816.

In the absence of any such reason or example, the premise of patentable distinctness has merely been restated as the conclusion for finding the same. Thus, the requirement to elect a single species of the claimed invention is improper and should be withdrawn.

Even if Applicant is somehow not entitled to examination of all of the pending claims, Applicant is certainly entitled to a complete examination of all of the method claims 1 and 3-15 in view of the complete lack of reasons and/or examples provided to support the requirement to elect a species of method claims.